

I Claim:

1. A method for adaptive channel equalization, which comprises:

providing a filter processing unit having a transfer function defined by a set of filter coefficients;

comparing a largest filter coefficient with a lower threshold value and an upper threshold value;

updating the filter coefficients in response to an error signal derived from an output signal from the equalizer and adjusting an output signal level of the filter processing unit by:

if the largest filter coefficient exceeds the upper threshold value, shifting bit sequences of the filter coefficients one bit position downwards and simultaneously shifting a bit sequence of an output signal from the filter processing unit one bit position upwards, and

if the largest filter coefficient is below the lower threshold value, shifting the bit sequences of the filter coefficients one bit position upwards and simultaneously

shifting the bit sequence of the output signal from the filter processing unit one bit position downwards.

2. The method according to claim 1, which comprises providing the filter processing unit with a plurality of processing stages; each of the processing stages:

providing a delayed signal by delaying an output signal from a preceding processing stage in a predetermined manner;

providing a multiplication result by multiplying the delayed signal by a filter coefficient; and

adding the multiplication result to an addition result from a preceding processing stage such that a subsequent processing stage is provided with an addition result.

3. The method according to claim 2, wherein one of the plurality of the processing stages multiplies an input signal by a corresponding filter coefficient and delivers a multiplication result to an adder in a second one of the plurality of the processing stages.

4. The method according to claim 1, which comprises:

for every filter coefficient, using a coefficient-updating stage to provide a delayed signal by delaying an output signal from a preceding coefficient-updating stage in a predetermined manner;

obtaining a multiplication result by multiplying the delayed signal by the error signal weighted by an update factor; and

adding the multiplication result to a stored value for a corresponding filter coefficient.

5. The method according to claim 4, which comprises:

supplying an addition result obtained in the adding step to coefficient-based shifters;

providing an output signal from the filter processing unit to a data signal shifter; and

if the largest filter coefficient exceeds the upper threshold value or is below the lower threshold value, supplying control signals to control inputs on the coefficient-based shifters and to a control input, which has an inverted sign, of the data signal shifter.

6. The method according to claim 4, wherein the delayed signal is multiplied by the error signal and by an update factor.

7. The method according to claim 6, which comprises independently adjusting the update factor for each coefficient-updating stage.

8. The method according to claim 7, which comprises:

in a first level-alignment phase, adjusting a magnitude of the update factor for each coefficient-updating stage based on magnitudes of the filter coefficients initially stored in corresponding coefficient-updating stages; and

in a second level-alignment phase, adjusting the magnitude of the update factor for each coefficient-updating stage to be identical to one another.

9. An adaptive equalizer, comprising:

a filter processing unit having a transfer function defined by a set of filter coefficients, said filter processing unit having an output;

a coefficient-updating unit having a plurality of coefficient-updating stages; and

a level-adjustment unit including:

a comparator for comparing a largest one of said filter coefficients with a lower threshold value and an upper threshold value,

a plurality of coefficient-based shifters having control inputs connected to said comparator, and

a data signal shifter at said output of said filter processing unit, said data signal shifter having a control input connected to said comparator.

10. The adaptive equalizer according to claim 9, wherein:

said filter processing unit has a plurality of series-connected processing stages; and

each of said plurality of processing stages includes:

a delay element for delaying an output signal from a preceding one of said plurality of processing stages,

a multiplier for multiplying a delayed signal by a corresponding one of said filter coefficients, and

an adder for adding an output signal from said multiplier and an addition result from a preceding one of said plurality of processing stages and for providing a subsequent one of said plurality of processing stages with an addition result.

11. The adaptive equalizer according to claim 10, wherein:

said multiplier of a first one of said plurality of processing stages is for multiplying an input signal by a corresponding one of said filter coefficients; and

said multiplier of said first one of said plurality of processing stages is connected to said adder of a second one of said plurality of processing stages.

12. The adaptive equalizer according to claim 9, wherein:

each one of said plurality of coefficient-updating stages includes:

a delay element for delaying an output signal from a preceding one of said plurality of coefficient-updating stages,

a coefficient memory connected to said filter processing unit,

a multiplier for multiplying a delayed signal by an error signal, said multiplier providing an output signal, and

an adder for adding the output signal from said multiplier and a value of one of said filter coefficients stored in said coefficient memory.

13. The adaptive equalizer according to claim 12, wherein:

said comparator has an output;

each one of said coefficient-based shifters has an input and an output, and a control input;

said coefficient memory has a plurality of inputs;

said adder of each one of said plurality of coefficient-updating stages has an output connected to said input of a respective one of said coefficient-based shifters;

said output of each one of said coefficient-based shifters is connected to a respective one of said plurality of inputs of said coefficient memory;

said control input of each one of said coefficient-based shifters is connected to said output of said comparator;

said output of said filter processing unit is connected to one of said coefficient-based shifters; and

said control input of each one of said coefficient-based shifters is connected to said output of said comparator.